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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/781,778 | 02/20/2004 | Kun-Hong Chen | SUND 502 | 3740 |

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RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

| EXAMINER | |
|---|---|
| WILSON, CHRISTIAN D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2891 | |

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/781,778 | CHEN, KUN-HONG | |
| | Examiner | Art Unit | |
| | Christian Wilson | 2891 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11022004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanabe *et al.*

Tanabe *et al.* (US 6,703,267) discloses a method for fabricating a low temperature polysilicon thin film transistor (TFT) comprising the steps of providing a substrate **1**, forming a polysilicon layer **502** on the substrate, forming a gate oxide layer **503**, forming a photoresist pattern and etching the polysilicon layer and gate oxide layer using the photoresist pattern [column 11, lines 35-45], removing the photoresist pattern [Figure 6(d)], forming a gate **505** on the gate oxide layer, and implanting dopants to form source/drain regions using the gate as a mask [column 11, lines 50-55].

Regarding claim 2, Tanabe *et al.* further discloses forming a buffer layer on the substrate prior to forming the polysilicon layer [column 11, line 18].

Regarding claim 3, Tanabe *et al.* further discloses forming a polysilicon layer with a thickness of 750 Å [column 11, line 17].

Regarding claim 4, Tanabe *et al.* further discloses forming a gate oxide layer with a thickness of 800 Å [column 10, line 3].

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe *et al.* in view of Kim *et al.*

Tanabe *et al.* teaches forming an aluminum (Al) gate, but does not discuss a molybdenum (Mo) or chromium (Cr) gate. Kim *et al.* (US 2003/0085404) teaches forming an Al, Mo, or Cr gate in a TFT [0042]. It would have been obvious to one of ordinary skill in the art to use Mo or Cr in the method of Tanabe *et al.* since these are well known substitute materials for the same purpose of forming a TFT gate.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe *et al.* in view of Suzawa *et al.*

Tanabe *et al.* teaches doping source/drain regions but does not discuss the dosage used. Suzawa *et al.* (US 2003/0116805) teaches a source/drain dopant dosage in a TFT of $1x10^{13}$ to $5x10^{14}$ [0093]. It would have been obvious to one of ordinary skill in the art to use the dosage of Suzawa *et al.* in the method of Tanabe *et al.* since this dosage provides an improved concentration gradient in the channel region [0011].

6. Claims 7 – 9, 12, 13, 15, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sera.

Sera (US 6,287,898) teaches a method of fabricating a TFT comprising the steps of forming a polysilicon layer **3** on a substrate **1**, forming a gate oxide layer **4** on the polysilicon

layer, forming a photoresist pattern on the oxide layer and etching the polysilicon and oxide layer [column 7, lines 1-5] to forming a first **17** and second **18** stack structure corresponding to two types of transistor, removing the photoresist pattern [Figure 5A], forming a gate **13** occupying a smaller region than the gate oxide layer, forming a source/drain region **7** by implating first heavy dopants **28** in the first type transistor and using a photoresist layer **19** to cover the second stack structure, implanting first dopants in the first type transistor to form the lightly doped region **11** using the gate as a mask [Figure 5E], forming source/drain regions **7** in the second type transistor by implanting second heavy dopants **29** using a photoresist layer **19** over the first stack as a mask. Sera teaches forming the heavily doped regions before forming the gate [Figure 5B]. It would have been obvious to one of ordinary skill in the art to form the gate first and then dope the heavily doped regions since Sera further teaches an alternate method of doping which uses the gate as a mask for heavy doping [Figure 6E] which provides simpler steps for forming the transistor [column 8, lines 45-60].

Regarding claim 8, Sera further teaches forming a buffer layer **2**.

Regarding claim 9, Sera further teaches forming an interlayer dielectric (ILD) **8**, selectively exposing the gates and source/drain regions [column 8, lines 10-15], and forming electrodes **9** to the gates and source/drain regions.

Regarding claim 12, Sera further teaches forming a patterned passivation layer **21** on the ILD and electrodes where the patterned passivation layer exposes a pixel area, and forming a transparent electrode **23** connected to the exposed portion of the electrode.

Regarding claim 13, Sera further teaches a transparent electrode of indium tin oxide (ITO) [column 18, line 20].

Regarding claim 15, Sera further teaches a gate oxide layer with a thickness of 800 – 1000 Å [column 7, line 65].

Regarding claim 20, Sera further teaches an NMOS and PMOS device [column 7, lines 5-20].

7. Claims 10 and 17 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sera as applied to claim 7 above, and further in view of You.

Sera teaches an interlayer dielectric layer and heavily and lightly doped regions, but does not discuss the ILD thickness or doping dosages. You (US 6,403,409) teaches an ILD with a thickness of 6000 – 8000 Å [column 5, lines 50-60] and light doping dosages of $1x10^{12}$ – $8x10^{13}$ ions/cm$^2$ and heavy doping dosages of $1x10^{15}$ – $5x10^{15}$ ions/cm$^2$ ions/cm$^2$ [column 4, lines 45-65; column 5, lines 1-15]. It would have been obvious to one of ordinary skill in the art to use the thickness and dosages of You since these provides a reduction in the damage to the polysilicon layer and omission of annealing and a typical ILD thickness for protecting the underlying devices.

8. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sera as applied to claims 7 and 9 above, and further in view of Kim *et al.*

Sera teaches forming a silicide gate, but does not discuss a molybdenum (Mo) or chromium (Cr) gate. Kim *et al.* (US 2003/0085404) teaches forming an Al, Mo, or Cr gate in a TFT [0042]. It would have been obvious to one of ordinary skill in the art to use Mo or Cr in the method of Tanabe *et al.* since these are well known materials for forming silicide gates in TFTs.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sera as applied to claim 7 above, and further in view of Tanabe *et al.*

Sera teaches a polysilicon gate layer but does not discuss the thickness of the layer. Tanabe *et al.* teaches forming a polysilicon layer with a thickness of 750 Å [column 11, line 17]. It would have been obvious to one of ordinary skill in the art to use a polysilicon thickness of

200 – 1000 Å since this range provides improved channel length/width and V-I characteristics [column 11, lines 60-67].

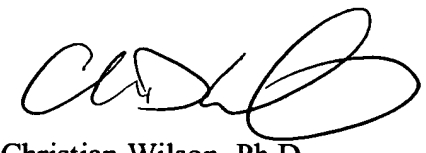
***Conclusion***

10. A copy of the search history is enclosed.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian Wilson whose telephone number is (571) 272-1886. The examiner can normally be reached on weekdays, 7:30 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Christian Wilson, Ph.D.
Primary Examiner
Art Unit 2891

CDW